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EXAMINER	
FLORES, LEON	
ART UNIT	**PAPER NUMBER**
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/731,850	Applicant(s) GUIMARAES, HOMERO L.	
	Examiner Leon Flores	**Art Unit** 2611	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. **Claims (1-3, 7, 16) are rejected under 35 U.S.C. 103(a) as being unpatentable over Baird (US Patent 6,204,787 B1) in view of Nonoyama et al. (hereinafter Nonoyama) (US Patent 6,529,015)**

Re claim 1, Baird discloses a sigma delta converter comprising: an integrator circuitry including an integrator input and an integrator output, wherein an input signal coupled to the integrator input has an input AC voltage component and a DC offset component (In Baird, see fig. 7A: 706 & 707, col. 7, lines 48-50); a pair of capacitors coupled to the integrator input (In Baird, see fig. 7A: 707a & 707b); a first set of switches coupled to the pair of capacitors, the first set of switches configured to transfer a first charge to the pair of capacitors during a first phase, the first charge proportional to a reference voltage (In Baird, see fig. 7B & col. 7, lines 59-61); and a second set of switches coupled between the pair of capacitors and the integrator input. (In Baird, see fig. 7B: 712a 712b)

But the reference of Baird fails to specifically teach that the second set of switches configured to transfer the first charge and a second charge to the integrator input, the second charge proportional to the DC offset component.

However, Nonoyama does. (See fig. 1: elements 3, 4, 5 & col. 6, line 18 – col. 7, line 6) In the same field of endeavor, Nonoyama discloses a second set of switches (switches a) configured to transfer the first charge and a second charge to the integrator input, the second charge proportional to the DC offset component.

Therefore, taking the combined teachings of Baird and Nonoyama as a whole. It would have been obvious to one of ordinary skills in the art to have incorporated theses features into the system of Baird, in the manner as claimed and as taught by Nonoyama, for the benefit of providing offset compensation.

Re claim 2, the combination of Baird and Nonoyama further discloses the sigma delta converter, as recited in claim 1, further comprising: a comparator coupled to the integrator circuitry output, the comparator including a comparator output. (In Baird, see fig. 4B)

Re claim 3, the combination of Baird and Nonoyama further discloses the sigma delta converter, as recited in claim 1, wherein the integrator circuitry comprises N integrators coupled in series forming an Nth-Order sigma delta loop filter, each of the N integrators having a first input, a second input, a first output and a second output, each of the N integrators having a first integrator capacitor coupled to the first input and the first output and a second integrator capacitor coupled to the second input and the second output. (In Baird, see fig. 4B & col. 6, lines 33-37)

Re claim 7, the combination of Baird and Nonoyama further discloses the sigma delta converter, as recited in claim 1, wherein the integrator is a continuous time integrator. (In Baird, see fig. 4B & col. 6, lines 34-37. Furthermore, since the signal is being integrated three times the signal is converted to digital until the last stage of the 3rd order modulator by an ADC.)

Re claim 16, the motivation for combining these two references has already been established in claim 1 above, therefore, the combination of Baird and Nonoyama further discloses a method comprising: during a first phase, charging a pair of capacitors to a

reference charge (In Baird, see fig. 7B & col. 7, lines 59-61); during a second phase, transferring a sum charge via the pair of capacitors to inputs of a first integrator (In Nonoyama, see col. 6, line 18 – col. 7, line 6) in a series of integrators in a sigma delta converter (In Baird, see fig. 4B), the sum charge including the reference charge and a DC offset correction charge. (In Nonoyama, see col. 6, line 18 – col. 7, line 6)

5. **Claims (4-6, 8, 17-18) are rejected under 35 U.S.C. 103(a) as being unpatentable over Baird (US Patent 6,204,787 B1) and Nonoyama et al. (hereinafter Nonoyama) (US Patent 6,529,015), as applied to claim 1 above, and further in view of Ferguson, Jr. et al (hereinafter Ferguson) (US Patent 6,040,793)**

Re claim 4, the combination of Baird and Nonoyama further discloses the sigma delta converter, as recited in claim 1, further comprising: a comparator coupled to the integrator circuitry output, the comparator including a comparator output (In Baird, see fig. 4B); wherein the polarity of the second charge is configured to cancel the DC offset component of the input signal. (In Nonoyama, see fig. 1 & col. 6, line 18 – col. 7, line 6)

But the combination of Baird and Nonoyama fails to teach a third set of switches coupled to the pair of capacitors, the third set of switches configured to change a polarity of the first charge and the second charge based on the comparator output; and a fourth set of switches coupled to the pair of capacitors, the fourth set of switches configured to change a polarity of the second charge based on the comparator output.

However, Ferguson does. (See col. 5, lines 5-12 & col. 6, lines 57-67) Ferguson discloses a third set of switches coupled to the pair of capacitors, the third set of

switches configured to change a polarity of the first charge and the second charge based on the comparator output (See col. 5, lines 5-12 & col. 6, lines 57-67); and a fourth set of switches coupled to the pair of capacitors, the fourth set of switches configured to change a polarity of the second charge based on the comparator output. (See col. 5, lines 5-12 & col. 6, lines 57-67)

Therefore, taking the combined teachings of Baird, Nonoyama, and Ferguson as a whole. It would have been obvious to one of ordinary skills in the art to have incorporated theses features into the system of Baird, as modified by Nonoyama, in the manner as claimed and as taught by Ferguson, for the benefit of providing offset compensation.

Re claim 5, the combination of Baird, Nonoyama, and Ferguson further discloses a digital to analog converter coupled to the pair of capacitors for producing the second charge. (In Ferguson, see col. 1, lines 63-64 & col. 4, lines 4-49)

Re claim 6, the combination of Baird, Nonoyama, and Ferguson further discloses that the digital to analog converter configured to receive a multi-bit code word input from a digital signal processor. (In Ferguson, see fig. 2: element 52, which include a DAC, is configured to receive a multi-bit code from element 78 in order to control the switches.)

Re claim 8, the combination of Baird, Nonoyama, and Ferguson further discloses that wherein the integrator is a discrete time integrator. (In Ferguson, see col. 1, lines

50-56. Furthermore, the output of the integrator clocked, latched comparator.)

Re claim 17, the combination of Baird, Nonoyama, and Ferguson further discloses comparing an output of a last integrator in the series of integrators to a zero value (In Baird, see fig. 4B. Furthermore, since the comparator located at the end of the third order sigma delta modulator has only one input, therefore, we can say that the other input is grounded.); and determining a polarity of the reference charge in the sum charge based on a result of the comparing. (In Ferguson, see col. 5, lines 8-12)

Re claim 18, the combination of Baird, Nonoyama, and Ferguson further discloses that wherein a polarity of the DC offset correction charge in the sum charge is independent of a result of the comparing. (In Nonoyama, see fig. 1)

Claims (9-10) are rejected under 35 U.S.C. 103(a) as being unpatentable over Baird (US Patent 6,204,787 B1) in view of Nonoyama et al. (hereinafter Nonoyama) (US Patent 6,529,015), and further in view of Bazarjani et al. (hereinafter Bazarjani) (US Patent 6,005,506)

1. Re claim 9, Baird discloses a radio frequency (RF) signal receive path comprising: an integrator circuitry including an integrator input and an integrator output, wherein an input signal coupled to the integrator input has an input AC voltage component and a DC offset component (In Baird, see fig. 7A: 706 & 707, col. 7, lines 48-50); a pair of capacitors coupled to the integrator input (In Baird, see fig. 7A: 707a &

707b); a first set of switches coupled the pair of capacitors, the first set of switches configured to transfer a first charge to the pair of capacitors during a first phase, the first charge proportional to a reference voltage (In Baird, see fig. 7B & col. 7, lines 59-61); and a second set of switches coupled to the pair of capacitors. (In Baird, see fig. 7B: 712a 712b)

But the reference of Baird fails to specifically teach that the second set of switches configured to transfer the first charge and a second charge to the integrator input, the second charge proportional to the DC offset component.

However, Nonoyama does. (See fig. 1: elements 3, 4, 5 & col. 6, line 18 – col. 7, line 6) In the same field of endeavor, Nonoyama discloses a second set of switches (switches a) configured to transfer the first charge and a second charge to the integrator input, the second charge proportional to the DC offset component.

Therefore, taking the combined teachings of Baird and Nonoyama as a whole. It would have been obvious to one of ordinary skills in the art to have incorporated theses features into the system of Baird, in the manner as claimed and as taught by Nonoyama, for the benefit of providing offset compensation.

The combination of Baird and Nonoyama discloses the limitations as claimed above, except they fail to specifically teach an intermediate frequency amplifier (IFA) including an IFA output; a plurality of anti-aliasing filters (AAFs) coupled to the IFA output, the AAFs having an AAF output; and a sigma delta converter coupled to the AAF output.

However, Bazarjani does. (See fig. 6 & col. 13, lines 41-61) Bazarjani discloses an intermediate frequency amplifier (IFA) including an IFA output (2426), a plurality of anti-aliasing filters (AAFs) coupled to the IFA output, the AAFs having an AAF output (2430a & 2430b); and a sigma delta converter coupled to the AAF output. (2440a & 2440b)

Therefore, taking the combined teachings of Baird, Nonoyama, and Bazarjani as a whole. It would have been obvious to one of ordinary skills in the art to have incorporated theses features into the system of Baird, as modified by Nonoyama, in the manner as claimed and as taught by Bazarjani, for the benefit of providing gain control, match filtering and/or anti-alias filtering, and to produce digitized baseband samples.

Re claim 10, the combination of Baird, Nonoyama, and Bazarjani further discloses the RF signal receive path, as recited in claim 9, wherein the integrator circuitry comprises N integrators coupled in series forming an Nth-Order sigma delta converter, each of the N integrators having a first input, a second input, a first output and a second output, each of the N integrators having a first integrator capacitor coupled to the first input and the first output and a second integrator capacitor coupled to the second input and the second output. (In Baird, see fig. 4B & col. 6, lines 33-37)

6. **Claims (11-15) are rejected under 35 U.S.C. 103(a) as being unpatentable over Baird (US Patent 6,204,787 B1), Nonoyama et al. (hereinafter Nonoyama) (US Patent 6,529,015), and Bazarjani et al. (hereinafter Bazarjani) (US Patent**

6,005,506), as applied to claim 9 above, and further in view of Ferguson, Jr. et al (hereinafter Ferguson) (US Patent 6,040,793)

Re claim 11, the combination of Baird, Nonoyama, and Bazarjani further discloses the sigma delta converter, as recited in claim 1, further comprising: a comparator coupled to the integrator circuitry output, the comparator including a comparator output (In Baird, see fig. 4B); wherein the polarity of the second charge is configured to cancel the DC offset component of the input signal. (In Nonoyama, see fig. 1 & col. 6, line 18 – col. 7, line 6)

But the combination of Baird, Nonoyama, and Bazarjani fails to teach a third set of switches coupled to the pair of capacitors, the third set of switches configured to change a polarity of the first charge and the second charge based on the comparator output; and a fourth set of switches coupled to the pair of capacitors, the fourth set of switches configured to change a polarity of the second charge based on the comparator output.

However, Ferguson does. (See col. 5, lines 5-12 & col. 6, lines 57-67) Ferguson discloses a third set of switches coupled to the pair of capacitors, the third set of switches configured to change a polarity of the first charge and the second charge based on the comparator output (See col. 5, lines 5-12 & col. 6, lines 57-67); and a fourth set of switches coupled to the pair of capacitors, the fourth set of switches configured to change a polarity of the second charge based on the comparator output. (See col. 5, lines 5-12 & col. 6, lines 57-67)

Therefore, taking the combined teachings of Baird, Nonoyama, Bazarjani, and Ferguson as a whole. It would have been obvious to one of ordinary skills in the art to have incorporated theses features into the system of Baird, as modified by Nonoyama and Bazarjani, in the manner as claimed and as taught by Ferguson, for the benefit of providing offset compensation.

Re claim 12, the combination of Baird, Nonoyama, Bazarjani, and Ferguson further discloses a digital to analog converter coupled to the pair of capacitors for producing the second charge. (In Ferguson, see col. 1, lines 63-64 & col. 4, lines 4-49)

Re claim 13, the combination of Baird, Nonoyama, Bazarjani, and Ferguson further discloses that the digital to analog converter configured to receive a multi-bit code word input from a digital signal processor. (In Ferguson, see fig. 2: element 52, which include a DAC, is configured to receive a multi-bit code from element 78 in order to control the switches.)

Re claim 14, the combination of Baird, Nonoyama, Bazarjani, and Ferguson further discloses that wherein the integrator is a continuous time integrator. (In Baird, see fig. 4B & col. 6, lines 34-37. Furthermore, since the signal is being integrated three times the signal is converted to digital until the last stage of the 3rd order modulator by an ADC.)

Re claim 15, the combination of Baird, Nonoyama, Bazarjani, and Ferguson further discloses that wherein the integrator is a discrete time integrator. (In Ferguson, see col. 1, lines 50-56. Furthermore, the output of the integrator clocked, latched comparator.)

7. **Claims (1 & 16) are rejected under 35 U.S.C. 103(a) as being unpatentable over Ferguson, Jr. et al (hereinafter Ferguson) (US Patent 6,040,793) in view of Nonoyama et al. (hereinafter Nonoyama) (US Patent 6,529,015)**

Re claim 1, Ferguson discloses a sigma delta converter comprising: an integrator circuitry including an integrator input and an integrator output, wherein an input signal coupled to the integrator input has an input AC voltage component and a DC offset component (See fig. 2); a pair of capacitors coupled to the integrator input (See fig. 2: C4 & C5); a first set of switches coupled to the pair of capacitors, the first set of switches configured to transfer a first charge to the pair of capacitors during a first phase, the first charge proportional to a reference voltage (See fig. 2: S13 & S16 & col. 6, lines 57-62); and a second set of switches coupled between the pair of capacitors and the integrator input (See fig. 2: S9, S10, S11, S12).

But the reference of Ferguson fails to specifically teach that the second set of switches configured to transfer the first charge and a second charge to the integrator input, the second charge proportional to the DC offset component.

However, Nonoyama does. (See fig. 1: elements 3, 4, 5 & col. 6, line 18 – col. 7, line 6) In the same field of endeavor, Nonoyama discloses a second set of switches

(switches a) configured to transfer the first charge and a second charge to the integrator input, the second charge proportional to the DC offset component.

Therefore, taking the combined teachings of Fergusson and Nonoyama as a whole. It would have been obvious to one of ordinary skills in the art to have incorporated theses features into the system of Fergusson, in the manner as claimed and as taught by Nonoyama, for the benefit of providing offset compensation.

Re claim 16, the motivation for combining these two references has already been established in claim 1 above, therefore, the combination of Fergusson and Nonoyama further discloses a method comprising: during a first phase, charging a pair of capacitors to a reference charge (In Ferguson, see fig. 2: S13 & S16 & col. 6, lines 57-62); during a second phase, transferring a sum charge via the pair of capacitors to inputs of a first integrator (In Nonoyama, see col. 6, line 18 – col. 7, line 6) in a series of integrators in a sigma delta converter (In Ferguson, see col. 2, lines 44-45), the sum charge including the reference charge and a DC offset correction charge. (In Nonoyama, see col. 6, line 18 – col. 7, line 6)

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leon Flores whose telephone number is 571-270-1201. The examiner can normally be reached on Mon-Fri 7-5pm Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LF
July 28, 2007

David Payne
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